

Applicant : Chinnugounder Senthilkumar et al.  
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Please amend the claims as follows (this listing of claims replaces all prior listings):

1. (Currently amended) ~~Circuitry for controlling the oscillating frequency of an oscillator, the circuitry~~ An apparatus comprising:  
a plurality of ~~drain-source connected MOSFET~~ capacitors, each of which is independently selectable by a control signal, and each of which provides a controllable amount of capacitance to ~~the oscillator to control the~~ an oscillator to control an oscillating frequency of the oscillator; and  
a bias circuit to provide a substantially constant voltage signal to bias at least one of the plurality of MOSFET capacitors.
2. (Currently amended) The ~~circuitry apparatus~~ of claim 1, wherein each of the plurality of capacitors has a different capacitance than the other capacitors, and a predefined amount of capacitance is provided by a predetermined combination of capacitors.
3. (Currently amended) The ~~circuitry apparatus~~ of claim 2, wherein the MOSFET capacitors ~~are comprise~~ comprise drain-source connected MOSFETs.
4. (Currently amended) The ~~circuitry apparatus~~ of claim 3, wherein the ~~MOSFETs are MOSFETs comprise~~ P-type enhancement mode MOSFETs.
5. (Cancelled) The circuitry of claim 3, wherein the MOSFETs are N-type depletion mode MOSFETs.
6. (Currently amended) The circuitry of ~~claim 1~~ claim 24 wherein the capacitors are selected from the group consisting of on-chip metal capacitors, on-chip poly capacitors, and discrete capacitors.

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7. (Currently amended) The ~~circuitry~~ apparatus of claim 1, wherein each of the capacitors corresponds to a transmission gate switch.

8. (Currently amended) The ~~circuitry~~ apparatus of claim 7, further comprising a set of memory registers to provide the control signals for selecting the individual capacitors

9. (Currently amended) The ~~circuitry~~ apparatus of claim 8, further comprising a set of buffer devices to decouple the transmission gate switches from the set of memory registers to prevent noise in the memory registers from passing to the capacitors through the transmission gate switches.

10. (Currently amended) The ~~circuitry~~ apparatus of claim 9, ~~further comprising a low pass filter connected to a direct current voltage supply to generate a filtered voltage signal in which the filtered power supply signal is used to power the set of buffer devices.~~

11. (Currently amended) The ~~circuitry~~ apparatus of claim 1, wherein the oscillator includes a resonator and an inverting amplifier.

12. (Currently amended) The ~~circuitry~~ apparatus of claim 11, wherein a first subset of the plurality of capacitors is selectively electrically coupled to a first terminal of the resonator, and a second subset of the plurality of capacitors is selectively electrically coupled to a second terminal of the resonator.

13. (Currently amended) An electronic device comprising:  
a real time clock to generate a real time clock signal, the real time clock having a digitally tunable oscillator that adjusts an operating frequency of the real time clock in response to digital control signals;

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a circuit to generate a system time signal based on the real time clock signal, the system time signal representing at least one of hour, minute, and second, ~~the real time clock having a digitally tunable oscillator for digitally adjusting an~~ the circuit to generate digital control signals to control the digitally tunable oscillator to adjust the operating frequency of the real time clock to speed up or slow down the system time signal; and

a memory device to store data representing a configuration of the digitally adjusted tunable oscillator.

14. (Previously presented) The electronic device of claim 13, further comprising a communication port for receiving a reference time signal that represents at least one of hour, minute, and second, wherein the digitally tunable oscillator is digitally adjusted according to the reference time signal to minimize the difference between the system time signal and the reference time signal.

15. (Original) The electronic device of claim 13, wherein the digitally tunable oscillator includes a capacitor bank having a set of capacitors with capacitance values in a binary-weighted relationship, the capacitors selectable through a set of control signals.

16. (Currently amended) A method comprising:  
generating a set of control signals to select a subset of capacitors from a set of capacitors;  
connecting the selected subset of capacitors to an oscillator;  
generating an oscillating signal using the oscillator and the selected subset of capacitors in combination; ~~[[and]]~~  
generating a system time signal using the oscillating signal, the system time signal representing at least one of hour, minute, and second; and  
adjusting the digital control signals to select a different subset of capacitors to adjust the oscillating signal to speed up or slow down the system time signal.

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17. (Original) The method of claim 16, further comprising receiving a reference time signal, comparing the reference time signal with the system time signal, and modifying the set of control signals in response to the difference between the reference time signal and the system time signal to select a different subset of capacitors.

18. (Original) The method of claim 17, further comprising saving data representing the setting of the control signals in a memory.

19. (Withdrawn) A method of generating a time signal comprising:  
generating a system time signal using a real time clock circuit that has a tunable oscillator for adjusting an operation frequency of the real time clock circuit;  
receiving a reference time signal over a network;  
adjusting the tunable oscillator to increase or decrease the operating frequency of the real time clock circuit in response to a difference between the system time signal and the reference time signal.

20. (Withdrawn) The method of claim 19 wherein adjusting the tunable oscillator comprises adjusting a set of control signals to modify a selection of a set of capacitors within a capacitor bank, the selection of the set of capacitors correlating to the operating frequency of the real time clock circuit.

21. (Withdrawn) Apparatus for providing a variable level of capacitance, comprising:  
a plurality of capacitors, each capacitor selectable through an independent control signal generated by a logic circuit, the selected capacitors providing an amount of capacitance that is the sum of the individual capacitances of the selected capacitors; and  
buffer circuitry for decoupling the plurality of capacitors from the logic circuit to prevent noise in the logic circuit from affecting the plurality of capacitors.

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22. (Withdrawn) The apparatus of claim 21, further comprising a filter circuit connected to a power supply to generate a filtered power supply signal that is used to power the buffer circuitry.

23. (Withdrawn) The circuit of claim 21, further comprising transmission gates, each of which corresponds to one of the plurality of capacitors and can be turned on by the independent control signal when the corresponding capacitor is selected.

24. (Currently amended) Apparatus comprising:

~~a control unit to control a real time clock signal, the control unit generating a set of control signals, each of which independently selects a capacitor from a plurality of capacitors, the selected capacitors being coupled to an oscillator, the selected capacitors in combination providing a controllable amount of capacitance to the oscillator to control the oscillating frequency of the real time clock signal; and~~

~~circuitry to generate a system time signal representing at least one of hour, minute, and second based on the real time clock signal.~~

circuitry to generate a system time signal representing at least one of hour, minute, and second based on a real time clock signal, the real time clock signal being generated by a real time clock having a plurality of capacitors that can be selectively coupled to an oscillator; and

a control unit to adjust the system time signal by generating a set of control signals to select a subset of the capacitors, the selected capacitors being coupled to the oscillator to provide a controllable amount of capacitance to the oscillator to control the oscillating frequency of the real time clock signal to speed up or slow down the system time signal.

25. (Original) The apparatus of claim 24 in which the control unit is disposed within a computer chipset.

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26. (Cancelled) The apparatus of claim 24, further comprising circuitry to generate the system time signal based on the oscillating frequency of the oscillator.

27. (Original) The apparatus of claim 26, further comprising a memory for storing the configuration of the set of control signals, and a data processing unit that processes data based on the system time signal.

28. (Previously presented) The electronic device of claim 13 in which the digitally tunable oscillator can be adjusted to oscillate at a frequency equal to 32768 Hz.

29. (Previously presented) The apparatus of claim 24 in which the plurality of capacitors include a subset of capacitors that, when coupled to the oscillator, causes the oscillator to oscillate at a frequency of 32768 Hz.

30. (Previously presented) The circuitry of claim 1 in which the bias circuit comprises a low pass filter connected to a voltage supply to generate a filtered voltage signal to bias the capacitors.

31. (Currently amended) The circuitry of ~~claim 4~~ claim 30 in which the filtered voltage signal has a voltage level sufficient to bias the P-type enhancement mode MOSFETs into saturation.

32. (Previously presented) The circuitry of claim 30 in which each of the capacitors has a first terminal selectively coupled to the oscillator and a second terminal coupled to the filtered voltage signal.

33. (Previously presented) An apparatus comprising:  
an oscillator; and  
a plurality of capacitors, each of which is independently selectable by a control signal, and each of which provides a controllable amount of capacitance to the oscillator to control an

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oscillating frequency of the oscillator, each capacitor comprising a drain-source connected MOSFET.

34. (Previously presented) The apparatus of claim 33, further comprising a low pass filter to generate a filtered voltage signal for biasing at least one of the capacitors.

35. (Previously presented) The apparatus of claim 33, further comprising a device that generates a time signal based on the oscillating frequency of the oscillator.

36. (New) An apparatus comprising:

a plurality of drain-source connected N-type depletion mode MOSFET capacitors, each of which is independently selectable by a control signal, the selected capacitors providing a controllable amount of capacitance to an oscillator to control the oscillating frequency of the oscillator, each of the selected MOSFET capacitors having a gate node that is coupled to the oscillator and a drain node and a source node coupled to ground.

37. (New) The apparatus of claim 36, further comprising a device that generates a time signal representing at least one of hour, minute, and second based on the oscillating frequency of the oscillator.

38. (New) The apparatus of claim 37, further comprising a control unit to generate a set of control signals to select a subset of the capacitors to control the oscillating frequency of the oscillator to speed up or slow down the time signal.